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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,665	11/26/2001	Takahiro Iijima	323-01	5728

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EXAMINER
WONG, EDNA

ART UNIT	PAPER NUMBER
1753	9

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,665	IIJIMA ET AL.	
	Examiner	Art Unit	
	Edna Wong	1753	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Specification

I. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the word "said" is used in lines 3. Correction is required. See MPEP § 608.01(b).

II. The disclosure is objected to because of the following informalities:

page 7, line 10, reference character "22" has been used to designate both the vias and the metal layer (from page 7, line 5). It is unclear what reference character "22" designates.

page 9, lines 10-11, reference character "40" has been used to designate both the resin layer and the multi-layer wiring board (from page 9, line 9). It is unclear what reference character "40" designates.

page 11, line 37, the words -- (not shown) -- should be inserted after "42, 42, ..".

page 12, line 1, the words -- (not shown) -- should be inserted after "16, 16, ..".

page 12, line 1, the words -- (not shown) -- should be inserted after the number "40".

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims **1-2, 4 and 6** are objected to because of the following informalities:

Claim 1

line 8, the words "applying an" should be deleted because the words "applying an electroplating" sounds awkward.

Claim 2

line 2, it is suggested that the word -- a -- be inserted after the word "by".

Claim 4

line 2, the word "steps" should be amended to the word -- step --.

Claim 6

line 10, the words "applying an" should be deleted because the words "applying an electroplating" sounds awkward.

line 25, the words "applying an" should be deleted because the words "applying an electroplating" sounds awkward.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims **4-5 and 7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4

lines 3-4, it is unclear what is the relationship between the wiring board (or

"forming pads" step) and the body (process steps) of claim 1 because the wiring board has antecedent basis in the preamble of claim 1.

Claim 5

line 5, it appears that the wiring patterns are the same as the wiring pattern recited in claim 1, lines 14-15. However, it is unclear if they are.

Claim 7

line 2, it appears that the resin layer is the same as the resin plate recited in claim 6, line 5. However, it is unclear if it is. Furthermore, it is unclear how the resin layer (from claim 6, line 19) is formed by a press-forming process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

I. Claims **1-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Odaira et al.** (US Patent No. 5,333,379).

Odaira teaches a process for manufacturing a wiring board, said process comprising the following steps of:

(a) making a resin plate having via through holes (= an electrical insulating resin having a *perforated* three-dimensional substrate structure);

(b) coating (= chemical plating) all of the surfaces of the resin plate with a metal film (= an electrical conductive metallic material layer is formed on the surface);

(c) electroplating using said metal film as a power-supply layer; and

(d) removing (= etching) said metal film formed on said resin plate, so that vias are exposed on a surface the same as that of said resin plate (= conductor circuits are arranged on the opposite surfaces of the wiring board such they are electrically connected to each other) [col. 1, lines 15-45].

Odaira does not teach wherein the resin plate has wiring pattern recesses.

However, the invention as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made because one skilled in the art would have been motivated to have modified the process of Odaira with wherein the resin plate has wiring pattern recesses because recesses such as cavities and trenches are conventional in the art to interconnect layers and components contained therein. This is well within the ordinary skill of the artisan dependent upon the intended use of the device, particularly to the environment to which the device will encounter, which would be most suited for the application of the device, absent evidence to the contrary.

As to wherein the coating includes inner walls of said wiring pattern recesses and via through holes; and wherein the electroplating fills a plated metal into said wiring pattern recesses and via through holes, Odaira teaches that conductor circuits are arranged on the opposite surfaces of the wiring board such *they are electrically connected to each other* (col. 1, lines 23-27). Thus, it appears that in order for the opposite surfaces of the wiring board to be electrically connected to each other, the via through holes ("*perforated*") would have been coated by the chemical plating and the electrical plating.

Furthermore, the inner walls of the wiring pattern recesses would have also been coated by the chemical plating and the electrical plating because these openings are the conducting circuits.

As to wherein the removing is except for the inner walls of said wiring pattern recesses and via through holes, this is well within one having ordinary skill in the art because these openings are the conducting circuits.

Furthermore, if the electrical conductive metallic material layer was left to cover the entire surface of the molded product, then the various structures would not be electrically isolated.

As to wherein said resin plate is formed by press-forming process; and wherein said resin plate is formed by an injection molding process, Odaira teaches molding (col.

1, line 31-36). Press-forming or injection molding is deemed conventional in the molding art and was not invented by the Applicants, unless proven otherwise. These techniques would have been doing the same endeavor in shaping the resin plate.

II. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Odaira et al.** (US Patent No. 5,333,379) as applied to claims 1-3 above, and further in view of **Tokuda et al.** (US Patent No. 5,870,289).

Odaira is as applied above and incorporated herein.

Odaira does not teach forming pads on one surface of the wiring board to which external connecting terminals are to be attached.

However, Tokuda teaches that connecting pads **11** of the integrated circuit chip **10** are connected to the wires **21** of the wiring substrate **20** through direct through-hole connections **40** (col.10, lines 42-47; and Fig. 1).

Thus, the invention as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made because one skilled in the art would have been motivated to have modified the process of Odaira by forming pads on one surface of the wiring board to which external connecting terminals are to be attached because this is conventional in the art to connect structures to the wires of the wiring

substrate as taught by Tokuda (col.10, lines 42-47; and Fig. 1).

III. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Odaira et al.** (US Patent No. 5,333,379) as applied to claims 1-3 above, and further in view of **Koyama** (US Patent No. 6,254,758 B1).

Odaira is as applied above and incorporated herein.

Odaira does not teach using said wiring board as a core substrate; and forming wiring patterns on the respective surface of the core substrate by means of resin layers to obtain a multi-layer wiring board.

However, Koyama teaches forming a multiple layer wiring board by the "buildup method" (col. 6, line 61 to col. 7, line 11).

Thus, the invention as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made because one skilled in the art would have been motivated to have modified the process of Odaira by using said wiring board as a core substrate; and forming wiring patterns on the respective surface of the core substrate by means of resin layers to obtain a multi-layer wiring board because forming a multiple layer wiring board by the "buildup method" would have not only formed a conductor pattern on a one-sided and on a two-sided wiring board but would have also

formed a conductor pattern on an inner layer of a multiple layer wiring board as taught by Koyama (col. 6, line 61 to col. 7, line 11; and Figs. 4 to 5(e)).

IV. Claims **6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Odaira et al.** (US Patent No. 5,333,379) in combination with **Koyama** (US Patent No. 6,254,758 B1).

Odaira and Koyama are as applied for the same reasons as discussed above and incorporated herein.

Citations

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uzoh et al. (US Patent No. 6,355,153 B1) is cited to teach a method for depositing a conductive material in the cavities of a substrate (col. 1, line 27 to col. 2, line 3; and Figs. 1A to 1C).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edna Wong whose telephone number is (703) 308-3818. The examiner can normally be reached on Mon-Fri 7:30 am to 5:00 pm, alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nam Nguyen can be reached on (703) 308-3322. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1495.

Edna Wong
Primary Examiner
Art Unit 1753

EW
September 3, 2003